Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

[0001] The present application is related to commonly owned and assigned Attorney Docket No. WIDC-021/00US, patent application no. 10/035,567, entitled *System and Method for DC Offset Compensation and Bit Synchronization*, which is filed on even date herewith and is incorporated herein by reference in its entirety. In this patent application, we describe a method that can be used to provide an accurate initial DC offset for the automatic DC tracker, thus improving the DC tracker's initial converge time and estimate stability. In the mean time, since the initial DC estimation is based on some known frame synchronization (sync) pattern, the method also performs and achieves frame detection. This patent application can therefore be applied to all wireless communications systems that use packet data with sync pattern in front.

Please replace paragraph [0004] with the following amended paragraph:

[0004] To implement Bluetooth and other such wireless protocols, a device receiving a transmitted signal is required to recover transmitted signal is required to recover transmitted bit patterns. The basic recovering process involves waveform demodulation, DC compensation, ~~but~~ bit synchronization and bit detection. Waveform demodulation usually is implemented in a radio module and is wireless protocol dependent. DC compensation can be implemented either in the radio module or in the baseband. It is a critical process, however, for achieving correct bit synchronization and detection. Bit synchronization and detection are usually implemented in the baseband and are common to many different wireless receivers. An automatic DC tracker and a bit synchronizer have been described in commonly owned and assigned patent application no. [_____] 10/035,567, filed October 22, 2001, Attorney Docket No. WIDC-021/00US.

Please replace paragraph [0013] with the following amended paragraph:

[0013] Moreover, using the $DC_{avg\_comp}(k)$, a bit slicer can be applied to determine the binary value (0 or 1) of the received sync pattern samples contained in DC_{sum}. That is, if the sample

value is greater than $DC_{avg\_comp}(k)$, it corresponds to a binary [)] 0, otherwise it is a binary 1. A correlator module can correlate the bit slicer output with the chosen portion of the known sync pattern to determine whether a potential frame detection has occurred. For example, when a threshold number of the received sync pattern bits--adjusted according to the DC_{avg_comp}--match corresponding bits in the known sync pattern, a potential frame detection can be declared.

Please replace paragraph [0020] with the following amended paragraph:

[0020] The frame detector module ~~150~~ 155 is configured to confirm a potential frame detection by the DC offset module 150. In the preferred embodiment, the frame detector module 155 confirms the frame detection based upon the last 30 bits of the Bluetooth synchronization word.

Please replace paragraph [0022] with the following amended paragraph:

[0022] The DC_{avg_comp} calculator 170 calculates the DC_{avg_comp} value used by the comparators. If the sampling rate results in N samples per symbol, the DC_{avg_comp} calculator 170 would use 34 x N running samples from the A/D converter 135. However, to reduce hardware complexity--by allowing bit shifting to replace complex multiplication--32 x N samples from the A/D converter 135 can be used to calculate the DC average ~~(DC_{avg})~~ (DC_{avg}) which can be approximated by

$$DC_{sum}(k) = \sum_{i=k-32xN+1}^{k} y(i)$$

$$DC_{avg}(k) = DC_{sum}(k) / (Nx32)$$
$$= (DC_{sum}(k) / N) >> 5$$

where k is the current sample time index and $y(i)$ is the output from the A/D converter 135. If $N = 4$, then

$$DC_{sum}(k) = \sum_{i=k-32x4+1}^{k} y(i)$$

$$DC_{avg}(k) = DC_{sum}(k) / (4x32)$$
$$= (DC_{sum}(k) / 4) >> 5$$
$$= DC_{sum}(k) >> 7.$$

Please replace paragraph [0024] with the following amended paragraph:

[0024] Still referring to FIGURE 4, the output from the individual comparators can be latched in storage devices, DC corrected symbol 0 through DC corrected symbol 33 (but do not necessarily need to be) and passed to a correlation module ~~165~~ 160, which compares the output of the individual comparators with the known synchronization word to identify a potential frame detection. A potential frame detection can be declared at any sample time assuming a threshold number of bits of the DC corrected samples--as stored in DC corrected symbol 0 through DC corrected symbol 33--match the corresponding bits in the known synchronization word.

Please replace paragraph [0025] with the following amended paragraph:

[0025] After a potential frame has been detected, the value for the DC_{avg_comp} (k) is frozen and the next symbol peak is identified by the peak ~~idetifier~~ identifier 165. For example, the correlation process could be continued for the next (*N-1*) samples to identify matching of the first 34 bits of the synchronization word. Assuming that the first 34 bit correlation match occurred at sample time n and *N=4*, the following rules can be used to determine the symbol peak location based on the correlation pattern over the four sample period (n to n + 3 ~~34~~):

1. If correlation matches occurred at both time n and n + 3 ~~34~~, regardless of what happened in between, the symbol peak is at n + 2;

2. If the only matches occur at time n, the symbol peak is at n;

3. If a correlation match occurred at time n + 3, and either time n + 1 or n + 2 or both also had correlation matches, the symbol peak is at n + 2; and

4. For all other cases, the symbol peak is at n + 1.

Please replace paragraph [0027] with the following amended paragraph:

[0027] The output from each latch is passed to the corresponding comparator 175 and compared against DC_{avg_comp}, which is an input to each comparator 175. The output from each comparator 175 is then passed to one of the correlation modules shown in FIGURE 6. For example, the outputs ~~B00, B10, . . . B320, and B330~~ b00, b10, ..., b330 are passed to correlator 0; the outputs ~~B01, B11, . . . B321, and B331~~ b01, b11, ..., b331 are passed to correlator 1; and so on. In other words, the first sample from each symbol storage is passed to a first correlation module, the second sample to a second correlation module, the third sample to a third correlation module, and the fourth sample to a fourth correlation module.

Please replace paragraph [0035] with the following amended paragraph:

[0035] Assuming that the threshold value has been crossed and branch 235 followed, the DC_{avg_comp} (k) for the current sample time is frozen (step 245) and a symbol peak is located (step 250). Assuming that the potential frame detection was declared at sample time n and *N=4*, the following rules determine the symbol peak location based on a continued correlation over the next five sample period (n to n + 4 ~~43~~):

1. If correlation matches occurred at both time n and n + 4 ~~43~~, regardless of what happened in between, the symbol peak is at n + 2;

2. If the only matches occur at time n, the symbol peak is at n;

3. For all other cases, if the symbol peak is at n +1 or ~~n = 2~~ n + 2 or both also had correlation matches, the symbol peak is at n + 2; and

4. For all other cases, the symbol peak is at n + 1.